Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT205 | Renewed embedded flash and other innovative NVM for extended domains of application [REFINED]

The CATRENE REFINED project aims to create fully integrated platforms for the embedding of non-volatile flash memory (NVM) functions in sub-90 nm CMOS technologies. Despite the complexity of the developments involved and the difficult economic situation, more and more companies worldwide are trying to enter the embedded NVM area. The principal objective of this major project is to maintain Europe leadership in the embedded NVM field and those major sectors which depend on it – such as smart cards, automotive controllers and consumer electronics. This requires not only solutions based on a technology-shrink path following Moore's law, but also low cost approaches and innovative cell concepts.

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	✔
Health and aging society	
Safety and security	✔
Energy efficiency	
Digital lifestyle	
Design technology	
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	✔
More Moore	✔
Technology node	< 130 nm

PROCESS DEVELOPMENT

Partners:

Atmel
CEA-LETI
Infineon Technologies
LFoundry Rousset
STMicroelectronics

Project leader:

Dominique Goubier
STMicroelectronics

Key project dates:

Start: January 2010
End: December 2012

Countries involved:

France
Germany
Italy

Non-volatile memory (NVM) technologies play a crucial role in developing reliable, high performance microcontrollers used in various applications including smart cards, the automotive sector and consumer electronics. There is now a notable effort in Europe to integrate NVM into baseline CMOS technologies, creating programmable product platforms for more generic system-on-chip (SoC) realisation and thereby increasing European chipmakers' competitiveness in derivative technologies.

Embedding flash memory in SoC devices answers the paradox between SoC requirements and mass production. A SoC is designed to satisfy a specific set of user requirements and so by nature is application specific. This inevitably limits volumes and hence is in contradiction with cost-efficient production. Embedded NVM technology facilitates the use of application-specific software in more generic SoCs, thereby combining volume production with product differentiation.

Meeting increasing demand

The CATRENE CT205 REFINED project aims both to create fully integrated technology platforms for the embedding of NVM functions in sub-90 nm CMOS technologies and to set up cost-effective solutions for qualified technologies. The goal is to meet the increasing demand for embedded NVM content in SoC devices that extends from a few kilobytes for security or personalisation up to several Megabytes for high-end automotive applications.

REFINED brings together major R&D actors – chipmakers and research organisations – to develop the 65/55 nm generation as well as improvements to the current 90 nm generation through technology shrink; it will also provide cost-effective solutions for qualified technologies – 150/110 nm. The base for the next generation is also set along evolutionary approaches as well as more radical ones. Essential issues of reliability, testing and IP development will be addressed in parallel.

It is further aimed at supporting the broad IP portfolio of the European project partners by reducing the time required to validate and industrialise new NVM cell concepts and process options. For this, REFINED will rely on close co-operation between its industrial partners and research centres, in which reuse of existing technology platforms for industrial validation of the new concepts and process options will be central.

Cross-European co-operation is prerequisite for successful completion of this challenging project as the knowledge and competences of the different partners are complementary and cannot be found within a single European country. The partners have already worked together in MEDEA, MEDEA+ and EU Framework Programme projects focused on embedded NVM and analogue process

options from 180 down to 90 nm baseline CMOS, with preliminary research into 65 and 45 nm cell concepts and process options.

This CATRENE project builds on this long European co-operation and the good results achieved so far. Parallel work is being carried out in the MEDEA+ MaxCaps project and in the more design-oriented SMART project in the ENIAC JU programme essentially based on phase-change memory.

Major innovations

Main innovations proposed in REFINED include:

- Integration of NVM options in deep sub-100nm standard CMOS technologies, without any performance degradation in the baseline CMOS;
- Integration of flash memory with 55 nm CMOS logic on 300 mm wafers;
- Bringing innovative cell options such as nanocrystals or process options like high-K dielectrics closer to industrialisation through close co-operation between the research and industrial partners;
- Development of new low-cost cell solutions aimed at overcoming the limitations of the existing technical offer, for example in terms of endurance, without increasing the overall process cost; and
- Development of test structures and methodologies to characterise and verify the analogue performance of the embedded NVM technology platforms.

The variety of solutions studied will enrich the European offer and capability to answer any possible market requirement. The final goal is to maintain and consolidate the leadership of European companies in offering the most advanced embedded NVM SoC solutions worldwide.

Well-recognised leadership

European leadership in embedded NVM is well recognised. In recent years, consortium partners have released the first embedded NVM products in the world for 180, 130 and 90 nm technology nodes. These were based on work in previous international co-operative projects. The target and present forecast is that STMicroelectronics should be able to be the first to announce the availability of a 55 nm embedded flash technology working with 300 mm wafers.

For products with a large memory-to-logic area ratio – such as subscriber identity module smart-card products for mobile phones – it is expected that 90 nm shrink technologies using 200 mm wafers will be very cost competitive with respect to 65 nm technology. Therefore Infineon is working on such an intermediate technology node within REFINED and expects to be the first in the industry able to offer such products.

For devices requiring a moderate NVM size allowing optimum stored information granularity demanded for applications targeting code access – such as nomadic applications, smart cards and industrial control – shrinking embedded single poly electrical erasable programmable read-only memory (EEPROM) at 150/130 nm while using 200 mm wafers is a very cost-competitive way forward. This will meet the demands from future customers not considering a high density embedded NVM because the application they target does not need it. ATMEL intends to develop this offer within the REFINED project.

High margin opportunities

Despite the increasing shift of manufacturing operations towards low cost areas of the world, the increase of added value in SoC products possible as a result of REFINED will allow European companies to be better positioned with respect to lower manufacturing cost areas. They will also be able to be more focused on innovative products that represent reliable, high margin opportunities.

Furthermore, with the participation of STMicroelectronics and CEA-LETI in the Grenoble area and Infineon in Dresden, REFINED will also strengthen co-operation between the Dresden and Grenoble nanoelectronics clusters initiated in March 2010. The CATRENE project is fully aligned with the goal of strengthening co-operation in advanced technologies and industrial processes that were agreed as areas of co-operation between the two clusters.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
Tel.: +33 1 40 64 45 60 - Fax: +33 1 45 48 46 81
Email: catrene@catrene.org
http://www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.