Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT305 | Development of 450 mm SOI substrates, related technologies and equipment [SOI 450]

CATRENE 450 SOI is developing silicon-on-insulator (SOI) substrates to bring equipment and substrates to a mature level of industrialisation for the transition to 450 mm silicon wafers. It aims to stimulate a European infrastructure which will lead the work in 450 mm development on SOI materials and related advanced technologies such as bonding, cleaning and thermal treatment. Work includes tool development and SOI implementation, with feasibility milestones, followed by the start-up of an initial processing line. The overall objective is to ensure Europe will be fully-prepared to participate and contribute actively to the wafer-size transition in this innovative and technology-driven market segment.

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	✔
More Moore	✔
Technology	<22 nm

MANUFACTURING SCIENCE: CROSS-CUTTING TECHNOLOGIES, EQUIPMENT AND MATERIALS

Partners:

Altatech
ASM
AVP
CEA-LETI
EV Group
Fraunhofer
IMEC
Intel
Mattson
SOITEC

Project leader:

François Brunier
SOITEC

Key project dates:

Start: November 2011
End: December 2014

Countries involved:

Austria
Belgium
France
Germany
Ireland

The worldwide semiconductor industry has been driven by Moore's Law for over 40 years. During that time, it has been determined that the benefits of reduced cost per transistor, better performance and increased functionality allow for increased budgets for innovative design. However, even assuming a very moderate cost increase in the range of 10 to 15% from generation to generation, it is easy to calculate that the cost/cm^2 doubles about every ten years. To re-establish reasonable manufacturing costs/cm^2, the industry has undergone a wafer-size transition about every eight to ten years.

The last wafer-size transition occurred at the beginning of this decade with the introduction of production lines with 300 mm diameter wafers. The next wafer-size transition is therefore imminent. The industry has already selected 450 mm as the new standard. The three major global semiconductor companies have been working together for two to three years to prepare for the next wafer size to achieve the necessary manufacturing cost reductions.

Since 2007, the International SEMATECH Manufacturing Initiative (ISMI) has collected and developed requirement guidelines, reusing many 300 mm wafer guidelines to leverage learning where existing concepts are proven. Early designs in 2007 transitioned to early wafer-handling prototypes in 2008 and an effort to produce a bank of 450 mm test wafers for equipment evaluation materialised in 2009. In 2010, ISMI was ready to accept process-equipment prototypes and commence demonstrations.

European activity on 450 mm wafer size will interact with the ISMI process, eventually contributing to a first 450 mm pilot line in 2012, as defined by the current International Technology Roadmap for Semiconductors (ITRS). The CATRENE CT305 SOI 450 project brings together the experience and expertise of leading European players in the semiconductor equipment and materials environment to ensure that Europe is fully-prepared to participate and contribute to the transition.

Powerful engine for growth

SOI 450 involves the development of equipment and materials for the next generation of semiconductor devices. These products define a huge, self-sustaining market by themselves. In these global markets, the European equipment and materials industry has achieved a world-leading position and acts as a powerful European engine for economic growth in its own right. The introduction of the 450 mm wafer diameter will be a new opportunity for the European equipment and materials industry to improve its competitiveness and gain market share.

More than 80% of silicon-on-insulator (SOI) substrates are manufactured by SOITEC, the global leader in this domain. Its success is largely attributed to strong collaboration with key European equipment suppliers and research laboratories. As SOI substrates are one key path to nanoscale CMOS, identified by end users for digital applications, system on-chip devices and memories, large volume applications are forecast at 450 mm. It is essential to capture this market with the transition to 450 mm.

This CATRENE project aims to stimulate the European infrastructure concerned with 450 mm development on SOI materials and related advanced technologies such as bonding, cleaning and thermal treatment. The objective is to increase European leadership within this highly innovative and technology-driven market segment. This target requires a joint effort for the development of innovative substrates and equipment.

Highly competitive

Currently, 450 mm standards are being established within SEMI and developments are being integrated with the ITRS, which indicates that the launch of the first 450 mm pilot lines will be in 2012.

European semiconductor equipment and materials companies have decided that, to secure their global business activities, they need to take an active part in these developments. Consequently, a European equipment and materials 450 mm initiative was established in 2009 under the umbrella of SEMI. The main goal is to maintain a high level of competitiveness for the European equipment and materials industry.

The innovation and technical challenges deal not only with the size change but also in the higher substrate quality needed for the ultimate nodes targeted by the wafer-size transition. These nodes will be more sensitive to contamination, requiring new specifications. New technologies and equipment will have to be developed to produce larger wafers for advanced CMOS technologies far beyond 22 nm.

Major objectives of SOI 450 are to ensure the fabrication of SOI substrates at the right moment for time to market, and develop new business opportunities. SOI offers a powerful tool to balance power efficiency and performance: it provides increased transistor switching speed of more than 30%, power reductions of 50% or a trade-off in power/performance and superior isolation for circuit and design. It also enables compact integration of intellectual property blocks. Furthermore, SOI will play a key role in the 'more Moore' race as it answers most of the scaling challenges. These ultimate nodes are the ones targeted by 450 mm transition.

The ambitious goals of 450 SOI can only be reached by intensified co-operation and sharing of expertise within Europe. Close collaboration between European material vendors, equipment and subsystem suppliers, as well as with academic partners, will promote an increase of the European market share and ensure a competitive position on the global market for 450 mm SOI material.

Europe stakes a claim

SOI 450, together with other European 450 mm projects, will have a significant impact on further R&D activities. It will provide access for the companies involved and European research institutes to the necessary 450 mm SOI technology. Without European and national funding, worldwide co-operation and the access to 450 mm would be very limited because a large part of the development work would then be performed in Asia or the USA.

Such projects are an important way for the European equipment and materials industry to participate in the next-generation wafer technology and in the worldwide market for 450 mm equipment and materials. It is envisaged that, because of their huge size, there will only be a small number of 450 mm high volume fabrication facilities built around the world. It is therefore very important that Europe stakes a claim to the possibility of having at least one such facility built and operated in the region.

CATRENE Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
Tel.: +33 1 40 64 45 60 - Fax: +33 1 43 21 44 71
Email: catrene@catrene.org
http://www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.