PROJECT PROFILE

2T102: High yield driven manufacturing excellence in sub-65 nm CMOS (HYMNE)

TECHNOLOGY PLATFORM FOR NEXT-GENERATION CORE CMOS PROCESS

Partners:

Air Liquide
Alcatel Vacuum
ALES
Atmel
Bede
CEA-LETI
Centre Microélectronique de Provence – Georges Charpak (CMP-GC)
CNRS-LTM
ELDIM
FEI
GeMeTec
ION-TOF
Jobin Yvon
MASA
M+W Zander
Netral
Philips
RECIF Technologies
R2D
SEZ
Si Automation
SOPRA
STMicroelectronics
Uni Eindhoven (TUE)
40-30

Project leader:

Joost van Herk,
Philips

Key project dates:

Start: 1 February 2005
End: 31 December 2008

Countries involved:

Austria
France
Germany
Italy
The Netherlands
UK

Increasing miniaturisation means electronics devices are becoming ever more difficult to produce at an industrial level. This is a particular problem in Europe where much of semiconductor manufacture is focused on often short-run, application-specific devices in a wide range of technologies. The MEDEA+ 2T102 HYMNE project has therefore set out to develop methods, software and hardware that will enable European chipmakers to shorten production cycle times and improve device yields, through increased automation and use of new materials. The result will be a significant gain in competitiveness in advanced technology manufacture, boosting global sales and improving European employment prospects.

Technology developments in the microelectronics industry are leading to ever smaller dimensions and ever greater complexity. Microelectronic devices with 65 nm features are already being developed and 45 nm devices studied. While this will result in new functionalities and applications for use in everyday life, it means devices are becoming more and more difficult to manufacture competitively.

Production challenges are particularly tough in Europe where chipmakers specialise in application-specific integrated circuits (ASICs) and application-specific standard products (ASSPs). Series production of such devices is much less than for the microprocessor and dynamic random access memory (DRAM) chips produced in high volumes in North America and Asia.

It is essential therefore to develop new smart equipment and process control strategies in Europe to meet very tight process margins for next generation devices at deep submicron levels – 65 nm node and below. Moreover, such advanced CMOS technology requires new materials, from high-k/low-k dielectrics to metal barriers, made with new deposition methods and chemical precursors. All this poses additional problems in terms of quality assurance and materials handling. In addition, introduction of so many new materials is certain to lead to serious process contamination, which again will affect yields.

Convincing customers

European chipmakers need to convince existing and potential customers they can provide advanced CMOS – and bipolar – technology reliably and predictably. And they must be able to guarantee delivery of high yield products with optimum cycle times at competitive prices, according to the challenges outlined in the International Technology Roadmap for Semiconductors (ITRS).

The MEDEA+ 2T102 HYMNE project has therefore set out to demonstrate it is possible to shorten development cycles for latest generation – less than 65 nm – complex CMOS technology and obtain device yields better than 78% within 13.5 months of first silicon out. In addition, it aims to analyse the wafer-fabrication process critically to reduce cycle times from two days to one per mask layer for standard items and from 0.75 days to 0.35 for fast prototyping in a running 300 mm fabrication plant. It also

intends to attain an additional five percent cut in defects as well as yield increases in the mature production/high volume stage. Consortium members include major device manufacturers STMicroelectronics, Philips and Atmel, materials producers such as Air Liquide, and suppliers of equipment, auxiliary hardware and software and facilities to the semiconductor industry such as FEI, SEZ, Alcatel Vacuum, Jobin Yvon, SOPRA and Si Automation, as well as several well-known European research centres and universities.

Key deliverables will include:

- Development and proof-of-concept of tools for capacity planning and controlled fab use to help improve efficiency and manufacturing flexibility;
- Well-characterised sources of materials and new precursor delivery systems necessary for successful introduction of new materials in 300 mm fabs and for volume production of products in sub-65 nm technology architectures;
- Understanding of the relationship between contamination induced by new materials and device yield, and measures to prevent and reduce the yield impact of such contamination; and
- Development of chemical and physical characterisation tools and associated analytical procedures needed to guarantee fast yield improvements and adequate fab control in time-to-market and time-to-volume phases.

Three parts

Project work will be split into three parts:

1. Factory management and automation. This will target implementation of advanced techniques to improve yield and cycle time by building a coherent framework to streamline management of volume production to reduce time to volume, and optimise introduction of new products and technologies to reduce time to market;
2. Supply of new materials and contamination-free wafer handling. This aims to cut the time for integration of new process modules, materials and chemistry for sub-65 nm CMOS production in high volume chipmaking. It will also involve facility development and tool-cleaning procedures to reduce wafer contamination. Innovative concepts will be developed and validated to enable contamination-free wafer handling in a 300 mm fab such as the shared Philips/STMicroelectronics Crolles-2 plant in France. New material precursors and slurries for chemical mechanical polishing will also be developed, validated and delivered with appropriate quality and volumes for 65 and 45 nm technologies; and
3. Zero-defect and advanced yield learning. This will involve examination and elimination of systematic and random defects for sub-65 nm technologies that could negatively affect yields. Such defects and contamination could result from new materials, processing tools and processing methods. The principal objective is to detect the various failure sources and modes early in the product life cycle to address processes and equipment problems and apply the appropriate wafer environment contamination control before production reaches high volume. Systematic process anomalies dominate yield in the early technology development phase as processes need to become mature and well controlled, whereas the remaining yield loss is primarily due to random defects generated in processing equipment, or present in wafer-storage units or in clean-room air. Mastering of yield requires development of two specific strategies: one for fast yield learning and the other for zero-defect manufacture.

Standard solutions will be pursued in the fields of automated process control, wafer handling and measuring protocols for exhausts, and contamination procedures and monitoring protocols. These will be major inputs for global standardisation, carried out by the Semiconductor Equipment and Materials Institute (SEMI).

Co-operation crucial

Vertical and horizontal co-operation being developed between chipmakers, materials, equipment and auxiliary hardware and software suppliers, and research institutes is crucial to the success of the MEDEA+ HYMNE project. It will also speed up dissemination of project results and benefit the overall manufacturing base for microelectronics in Europe.

Building up manufacturing know-how is essential to allow the European microelectronics industry and its suppliers to survive and to ensure job creation. The know-how resulting from this project is indispensable for the introduction of new technology in a controlled fashion with high yield. And it will provide the manufacturing excellence essential to enable European chipmakers to maintain and strengthen their position, while ensuring European suppliers have better chances to compete at a global level.

MEDEA+

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.