PROJECT PROFILE

A502: Multi-processor embedded systems architectures (MESA)

DESIGN METHODOLOGIES

Partners:

Adelante Technologies
Alcatel-Bell
Alcatel-Microelectronics
Bull
Coware
EDSN
IMEC
INRIA
LIP6/Uni Paris
Metasymbiose
Philips
Polyspace
STMicroelectronics
Uni Grenoble/TIMA
Uni Leuven (KUL)
Uni Nantes

Project leader:

Philippe Garcin,
STMicroelectronics

Key project dates:

Start: January 2001
End: December 2004

Countries involved:

Belgium
France
Italy
The Netherlands

Efficient design methods are urgently needed for reconfigurable multi-processor architectures. These will harness the huge computational capabilities of the 100-nm integrated circuit generation to exploding market demand in areas such as mobile communications, multimedia and high-speed data processing. Today, when a multi-processor architecture is targeted, no satisfactory solution is available for analysing the application area, defining communications protocols and validating the resulting solution. In the four-year MEDEA+ A502 MESA project, a consortium of 18 partners aims to fill this gap by providing flexible solutions for multi-processor architecture design covering a broad spread of applications.

While system-on-chip (SoC) design has to date focused on single or tandem processor solutions, the implementation of future electronic systems requires more complex architectures. These may include several processors and specific hardware blocks, organised around a communications structure and with distributed memory. However, extending architecture design automation from single- to multi-processor-oriented systems is a major task, requiring innovation in a number of areas.

Some existing tools are available to target complex multi-thread software written in a system specification model to a set of processors. Unfortunately, these approaches cannot be scaled for hardware/software multi-processor architectures, especially if these are to be integrated on a single chip. Global weaknesses in tool integration and functionality also necessitate a great deal of manual work in application development.

Device complexity and the increasing amount of embedded software in systems demand new ways of reducing delays in system validation. System prototyping currently remains a tedious process, requiring the development of additional models and the allocation of effort to support the realisation and debugging of a prototype on a target simulation platform. Penetration of formal methods for property checking in industry is still very limited, with the large size of the circuits being a major issue.

New design methods

A completely new generation of system design methods is required to permit the integration of heterogeneous components. Several key aspects must therefore be addressed:

- **Refinement in models** A multi-step methodology is needed to go from design analysis to implementation. These actions are tightly linked to mapping (how to split the design to minimise inter-block communication) and to partitioning (how to dispatch the blocks between hardware and software), which are still lacking satisfactory approaches;
- **Inter-processor communications** This area is also crucial. Two main approaches can be identified: reducing the volume of data exchanged between design blocks; and increasing the bandwidth of on-chip communication channels. Breakthroughs are needed in these areas, paying careful

attention to both hardware and software aspects; and

- **System verification** Specific validation platform architectures have to be investigated for system prototyping. Formal verification also needs to be studied as an alternative to classical methods. Through a mixed approach between formal methods and classical simulations, various trade-offs have to be proposed between flexibility, thoroughness and speed.

Powerful team

To address challenges of this magnitude, the MEDEA+ A502 MESA project brings together a powerful consortium co-ordinated by SoC supplier STMicroelectronics. Leading industrial partners provide a rich mix of applications experience: Alcatel in telecommunications terminals, Bull in computers, EDSN in digital radio networks and Philips in consumer electronics. These are joined by a group of SMEs active in computer-aided design (CAD), and by several leading European research institutes.

Most members of this team were involved in the earlier MEDEA SMT project, which dealt with single-processor systems. This demonstrated the effectiveness of such broad collaboration by developing a consistent set of 18 marketable CAD tools, stimulating four company start-ups and creating more than 110 new jobs. The successful methodologies employed in this initiative will continue to be applied within MESA.

The industrial partners forming the core of the MEDEA+ project are working together to ensure the complementarity of their offer and to provide development guidelines to the CAD participants. In addition, they head a series of vertical co-operations, from which further horizontal links will be spawned.

The variety of applications to be covered means that a single solution will not be able to meet a sufficient range of customer requirements. The project is therefore following a very pragmatic approach:

- Developing a super-toolbox consisting of generic tools. Each new CAD environment will be driven by industrial test cases that will demonstrate the validity of the method. Among other areas, consumer video terminals, hearing aids, data processing, video and speech processing, digital handsets with image reception, and broadband telecommunications will provide demonstrators; and
- Proposing platforms in response to specific needs: these platforms may be application-driven (e.g. software radio, audio) or communication-driven (e.g. switched packets). No MESA platform will be strictly processor-oriented. Instead, wide categories of processors will be distinguished (e.g. for multimedia).

Interoperability of these tools will be possible thanks to widely accepted standards such as SystemC – an initiative in which consortium partners will actively participate. Focusing on generic tools and platforms will allow European systems houses to compete successfully with US rivals in these areas.

Thanks to the critical mass provided by this consortium, both in terms of knowledge and experience, on-going interaction between CAD developers and potential users will ensure the relevance and timeliness of MESA outputs. In some areas of particular commercial sensitivity for Europe, market introduction of products based on the results of the project could be envisaged in the short term.

Growth markets

The single largest outlet for embedded-system IC components is digital cellular handsets, with average annual growth of 65% and almost 40 million handsets manufactured each year. Europe currently enjoys a strong position in this technology, as well as in the consumer and data processing sectors, where integrated system design is equally important.

With their newly acquired knowledge, the partners will be well placed to serve healthy future markets for both application-specific integrated circuit (ASIC) devices designed for a specific customer, and application-specific standard products (ASSPs), which meet the needs of multiple users.

Overall consumption of ASICs is predicted to increase at an annual rate of 20%, while the demand for ASSPs is expected to grow by an impressive 30% a year.

In addition to internal exploitation of the results, consortium members will disseminate know-how through publications, participation in public events such as European conferences, organisation of specialised training workshops for European designers and contributions to courses for industry.

As in the earlier MEDEA SMT project, partners will also continue to promote the emergence of start-ups in the electronic design automation field, and seek to generate new business that will bring additional employment in teams working on system-level issues.

MEDEA+ Office
33, Avenue du Maine
Tour Maine-Montparnasse
PO Box 22
F-75755 Paris Cedex 15, France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

EUREKA Σ!

MEDEA+ Σ!2365 is the new industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.