PROJECT PROFILE

A503: Advanced solutions for SoC innovative testing in Europe (ASSOCIATE)

DESIGN METHODOLOGIES

Partners:

Alcatel
Alcatel Microelectronics
INESC
Infineon
LIRMM
Philips Semiconductors
Tecmic
Temento

Project leader:

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Alcatel Microelectronics

Key project dates:

Start: July 2001
End: June 2004

Countries involved:

Belgium
France
The Netherlands
Portugal

The evolution of electronic technology towards higher integration levels imposes new challenges in the debugging and testing of products. There is considerable pressure to reduce the cost and time devoted to testing, even in the face of rapidly increasing design complexities. Current methods and tools are inadequate for modern development based on the creation and application of reusable, interoperable blocks of intellectual property (IP). The goal of MEDEA+ project ASSOCIATE is to streamline debugging and testing throughout the product life cycle, and to provide cost-effective methods appropriate to high-volume production – thus securing the competitive power of key European industry sectors.

The electronics market – especially in telecommunications, automotive, information technology, wireless communications and multimedia – is fast growing and intensely competitive, with a very high innovation rate. European industry can only maintain and increase its share by releasing cost-effective products with a short time-to-market.

The very high complexity of such products means that design for test (DfT), design for debug (DfD) and test application assume ever-greater importance in the overall development/production cycle.

According to the International Technology Roadmap for Semiconductors (ITRS), test costs have risen to a point where they may account for over 35% of the total expenditure for a complete system-on-chip (SoC) integrated circuit. This is a conservative estimate, and the proportion is expected to move still higher.

Time and performance pressures

Testing is not only expensive; both test development and testing during manufacturing are also becoming progressively more time-consuming. This trend must be reversed when market windows are shrinking, and manufacturers are under great pressure to adapt products' feature sets rapidly in response to evolving customer expectations.

Moreover, the ITRS also predicts that the test requirements for new process technologies coming on-line in the next two years will have outstripped the performance capabilities of the available automatic test equipment (ATE) systems, due to higher pin counts, speeds and memory volume. This implies the development of new SoC debug and test methodologies and tools that will enable product development, delivery and high quality levels to be achieved faster and at an acceptable cost.

Current scan-based test methods for high-complexity SoCs, including application-specific integrated circuits (ASICs) with mixed digital/analogue signal functions, can no longer cope with the complexity and newer technologies in an adequate and economical way.

Similarly, the current scattered and ad-hoc debug methodologies cannot deal with large IP-based SoCs. Multi-processor chips, in particular, pose new problems in debugging – so lead times for functional verifica-

tion and debug of SoCs take up an increasing part of the development time and cost. Therefore an important aspect of research lies in improving the controllability and observability of the internal logic of the ASIC, as a stand-alone device as well as in a complete system context. ATE test program development is on the critical path of product development. This task is becoming more and more difficult, due to soaring amounts of data to be handled and the resultant increase in ATE complexity. Fully integrated solutions for mixed-signal test program generation do not exist. Therefore, improvements are equally necessary in this field.

Cost-effective solutions

The objective of the MEDEA+ A503 ASSOCIATE project is to shorten debugging and testing times for the new devices, and to provide affordable testing methods that will be compatible with their production at high volumes.

Consortium leader Alcatel Microelectronics together with partners Alcatel Bell, Infineon and Philips have played leading parts in the development and manufacturing of complex SoC solutions in the telecommunications and multimedia domains. They are complemented by systems house Tecmic and tool development company Temento, an SME founded in 1995 and the only European commercial company of its kind, as well as academic members INESC and LIRMM.

Together, the team proposes to cover the whole product life cycle, from high-level design to prototyping and high-volume production, as well as defining computer-aided design (CAD) environments and conducting academic research.

Specifically, the aims of the project are to:

- Accelerate test program creation and test execution by developing test provisions on silicon (DfT). The methodologies will embrace testing for connections (structural testing) as well as performance – such as delay faults – through a general-purpose test access mechanism. Additionally, tools will be developed to provide an efficient DfT flow for various test solutions – built-in self-test (BIST), for example – and functional blocks such as memory and mixed-signal. The high integration level of future products makes this work necessary because external testers provide insufficient data bandwidth for a complete test. At the same time, the new approach will reduce the silicon overhead for testing;
- Reduce silicon debugging time by adopting a systematic approach to DfD. Special attention will be paid to multi-core debugging and a generic test equipment interface. Additionally, automatic tools will be developed to add observability and controllability to the internal IP in SoCs, and to support the debugging process. This will significantly speed up the debugging process. The consortium intends that the innovative work carried out under ASSOCIATE should form the basis of an international standard. The driver is that debugging a multi-million-transistor SoC creates a serious time-to-market bottleneck; and
- Make test application more effective by developing a coherent system-level design method for test program development and performance tests for time-critical designs such as high-speed mixed-signal blocks. Introducing tools that automate parts of the test program generation and provide portability of the programs across different ATE platforms will permit efficient test application. These applications will bridge the gap between CAD and ATE, and allow fast implementation of at-speed and performance tests, using advanced but still low-cost test equipment.

Building project synergy

ASSOCIATE benefits from previous European co-operation in a number of projects under the previous MEDEA programme and other nationally funded initiatives. In addition, it has links with the current MEDEA+ A208 (technology for reconfigurable intellectual property [TRIP]) and T101 (technology-driven design and test for system innovation on silicon [TechnoDat]) projects. In TRIP, testability and debug is a minor activity related to the specific application of re-configurable hardware. TechnoDat addresses the testing of digital standard cells and embedded blocks, together with design techniques for very-deep-sub-micron processes. As ASSOCIATE focuses on generic solutions for DfT, DfD and test application, a high level of synergy exists between these three projects.

The emerging tools will be able to handle very large and heterogeneous circuits with a high degree of accuracy down to the sub-micron and sub-nanosecond level. This is not only to produce dense designs, but also to provide for the efficient means of debugging and testing that are crucial to the future of the European microelectronics industry.

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