PROJECT PROFILE

A509: Microelectronic EMC system design for high density interconnect and high frequency environment (MESDIE)

DESIGN METHODOLOGIES

Partners:

Alcatel SEL
AMG
Conti Temic
EADS
Fraunhofer Institute
Infineon Technologies
INSA/DGEI
Magneti Marelli
Nokia
Philips
Politecnico di Torino
Robert Bosch
STMicroelectronics
University of Paderborn
WIDIS
Zuken

Project leader:

Werner John,
Fraunhofer Institute

Key project dates:

Start: January 2001
End: December 2003

Countries involved:

France
Germany
Italy
The Netherlands

Semiconductor manufacturers continuously provide faster, more cost effective and more highly integrated devices. Current 2 GHz clock frequencies are expected to reach 10 GHz in 2012 – and design dimensions will have been reduced to 0.05 µm by the end of the decade, compared with 0.12 µm today. Chip area and component density will have increased with edge lengths of 40 mm against the current 20 mm. With such changes in performance and complexity, electromagnetic compatibility and parasitic emissions become ever more significant. MESDIE is providing a coherent approach to overcoming these problems at both chip and high-density packaging levels for the benefit of the European microelectronics industry.

Introduction of new submicron technology and higher packaging density on the subsystem level has led to greater customer demand for high-quality semiconductor devices. Semiconductor manufacturers and their application customers now have to deal with constraints on the chip level to meet electromagnetic compatibility (EMC) requirements of systems and subsystems and are therefore searching for suitable solutions. Due to continuous miniaturisation, higher clock frequencies, faster edge rates and more functionalities, the electromagnetic emission (EME) problem is causing more and more trouble for semiconductor manufacturers in various application areas, such as automotive, multimedia, telecommunications and computing facilities.

Satisfactory EMC microelectronic system designs that eliminate electromagnetic interference in electronic systems and an appropriate design methodology for integrated circuits (ICs) are crucial. Therefore methods and tools for an improved system design taking into account the boundary conditions and appropriate integration into design processes will be a major challenge for the global electronics industry in this decade.

Taking a model approach

In order to achieve higher performance, microelectronic components and subsystems are moving towards ever increasing miniaturisation. This requires improved functionality of the substrate and high density interconnect (HDI)/high density packaging (HDP), as well as the integration of passive elements, EMC protection devices and optimised interconnect systems.

As wiring demands and density increase, high density interconnect structures become an essential requirement for wireability. This can be handled by either the use of new packaging strategies – such as single chip package (SCP), multi-chip module (MCM) or single chip module (SCM) – or by extending existing standard packaging technologies.

Modelling is an important feature of the entire MEDEA+ A509 MESDIE project, which brings together the major European semiconductor manufacturers, systems houses and R&D institutes with different backgrounds in technology and design methodologies to develop a common European strategy on handling radio-frequency EMC (EMC/RF) susceptibility.

The modelling aspects have to be handled on three levels:

1. The electromagnetic emissions of ICs;
2. Susceptibility at chip level; and
3. New high-density interconnect structures.

MESDIE is therefore developing EME modelling and simulation, methods for modelling and simulation of susceptibility at chip level and new high density interconnect structures to deal with electromagnetic parasites simultaneously on both chip and high-density packaging levels.

In addition, the MESDIE partners are covering tool environment and design flows, rule development, diagnosis and validation on chip and HDI levels, as well as testing issues, such as the characterisation of chip and HDI parameters.

To meet these challenges, the MESDIE project intends to:

- Close the gap between IC-level design and application in terms of new hierarchical system design approaches and high density interconnect technology;
- Achieve higher performance and more compact electronic equipment in relevant applications, such as automotive, telecommunications and consumer electronics; and
- Obtain a design methodology for the information-network-based society of the future.

Parasitic electromagnetic effects – such as reflections and crosstalk on interconnects, delta-I-noise within the power supply system, the threat of electrostatic discharge and ambient pollution by electromagnetic fields – will all be considered in the design process together with conventional design constraints.

Shortening design cycle

It is a common goal of all project partners and internal as well as external customers to establish a strong link between design-dedicated methodologies capable of dealing with on- and off-chip EMC/RF issues. Appropriate improvements at all design levels will be obtained and translated into a shortening of the overall design cycle. These improvements will apply to the specific product portfolio of each project partner.

Shorter design cycles together with increased EMC demands force semiconductor manufacturers to adopt design strategies that avoid EMC-related redesigns. The strong demand for right first time EMC behaviour can only be achieved by EMC simulation during the design phase. Simulators such as those used for functional and timing correctness will soon also have to account for EMC effects.

Focusing the resource competences of the companies and research laboratories involved in MESDIE will ensure the success of the project and the project partners.

The Fraunhofer Institute for Reliability and Micro-integration (IZM) is carrying out the overall co-ordination and management of this MEDEA+ project.

Enabling the European microelectronics industry to provide circuit models and simulation techniques for parasitic behaviour simulation will lead to more cost effective and competitive designs in the worldwide semiconductor market..

Improving competitiveness

Results and applications from previous JESSI and MEDEA projects improved the international competitiveness of several partners. The MESDIE consortium therefore expects an additional improvement in the market position of European companies as a result of this MEDEA+ project. The approach proposed will enable users of chip products to develop complex systems more easily and with a shorter time to market. This will give the systems houses and semiconductor manufacturers in Europe the opportunity to be more competitive and to address a larger market.

Two fundamental principles are imposed in this project: the results of the public funded projects should lead to a benefit for industry; and the knowledge gained must be transferred to users from industry as well as to users within research institutes and universities. These requirements are being covered by a web-based project server, which will be continuously updated during the project, allowing for continuous monitoring of the internal co-operation and the transfer performance.

Due to the participation of research institutes and universities and their intensive co-operation with the MESDIE industry partners, training of the design engineers will be guaranteed.