PROJECT PROFILE

TI02: Application specific design for ESD and substrate effects (ASDESE)

ENABLING IC TECHNOLOGIES FOR APPLICATIONS

Partners:

Alcatel Microelectronics
Atmel Germany
Robert Bosch
Cadence Design Systems
Fakultat fur Elektrotechnik, University of Bochum
Fraunhofer Institute for Reliability and Microintegration
Fachhochschule, University of Osnabrück
IMEC
IMMS
Infineon Technologies
Institute for Microelectronic Systems (IMS), University of Hanover
Institute for Solid State Electronics (ISSE), Vienna University of Technology
Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH)
Melexis
Philips Semiconductors
STMicroelectronics
X-FAB

Project leader:

Wolfgang Wilkening,
Robert Bosch

Key project dates:

Start: April 2001
End: March 2003

Countries involved:

Austria
Belgium
France
Germany
Italy

Robustness against electrostatic discharge (ESD) and control of feedback via substrate coupling are becoming decisive competences for first silicon success. This is due to decreasing sizes, increasing complexity and higher operation frequencies. Insufficient control of these effects is very costly and time consuming to eliminate if their influence is only detected after the first wafers have been processed. Therefore ASDESE is developing methodologies to simulate the influence of ESD and substrate effects during the design phase, so designers can apply the necessary changes at this stage or integrate protective measures instead of redesigning the chip after a costly silicon learning cycle.

European chipmakers have a good position in the application-specific IC (ASIC) market. They want to keep this position even if the complexity of chips is still increasing and more and more different functions have to be integrated on one chip. Despite these challenges, the time to market for new devices is decreasing so that demand for first-time-right is very strong.

As a consequence, chip producers cannot afford to detect malfunctions only after testing of processed wafers and then to start redesigning – a mask set for a 0.18 micron process costs around € 250,000 and this figure will continue escalating for future generations. Therefore it is essential to detect and eliminate design failures and deleterious influences such as electrostatic discharge (ESD) or substrate effects during the design phase.

Rising to technical challenges

Over the past few years, much effort has been made to minimise the number of redesigns. However, ESD and substrate effects can still damage ASICs and are today major causes for redesign.

This is going to get worse as miniaturisation increases even further and chips have to operate at ever-higher speeds. Miniaturisation of devices on chips leads to higher sensitivity of these devices to ESD; thinner gate oxides especially require new protection measures. Designers are able to integrate more and more circuits of different functionality on a single chip. Problems will appear when undesired coupling between these circuits across the substrate occur. The trends for ever-higher operating frequencies – such as for radio-frequency devices – and lower supply voltages for hand-held systems only make these problems worse.

In some cases, a multi-chip solution can be an alternative. But for the rest, it is necessary to get round the problems using a single chip and making sure different 'mixed-signal' system functions do not conflict.

Timing behaviour and functionality are dominated not only by the size of devices such as transistors and resistors, but more and more by the number and dimension of the necessary interconnect lines. Metal interconnection is needed to link components, as well as providing a vehicle for transporting signals over long distances. Coupling between interconnect lines, and substrate noise, will lead to parts of the circuits malfunctioning.

It is therefore crucial at an early stage of circuit design to model the effects caused by coupling the substrate areas and interconnection layers together to find out how these elements can be shielded effectively and the substrate contacts work efficiently.

Establishing project goals

The goal of the MEDEA+ T102 ASDESE project is to improve the way of developing ASICs by simulation-guided design methods. Establishing a methodology that improves the way ASICs are designed right from the very first stage will make chips inherently more reliable. It will make it possible to get a more robust product to market quicker and so reduce the need for unnecessary, and costly, modifications and redesigns that currently occur in design and fabrication. This is especially important in the communications sector and for safety critical applications in the automotive industry.

ASDESE aims to design and produce new test structures and circuits, and evaluate them using a variety of computer simulation techniques. The behaviour of transistors and other integrated structures should be predicted reliably without silicon by a chain of software tools that simulate how the process, device and circuit behave. In addition to the classical human body model ESD, the project will focus on charged device model stress.

While software exists for modelling substrate coupling, it is not proven for productive designs. Therefore, the project aims to develop necessary new software and integrate it into the conventional design flow process to make it more effective. Available tools cover a wide range of very different requirements – from low to very high frequencies, from very accurate simulations with a limited number of pins to simulations with high numbers of nodes and large distances. An important goal of this project is to define a common interface for substrate simulation tools within a widely used design environment, making it possible to choose a tool that fits the design problem.

Partners pool experience

Project partners expect to apply the methods they have developed to their different technologies – deep sub-micron, smart power, silicon-on-insulator and high frequency processes such as BICMOS, bipolar and silicon germanium (SiGe). They bring know-how of ASIC design in automotive and high frequency applications, where they have to produce fully functional, complex circuitry on the first silicon – and on time – to an extremely demanding market. Preventing rework/redesign during the circuit design and processing stages is crucial if they are to remain competitive.

The consortium consists of 18 organisations – a group of semiconductor companies that covers Alcatel Microelectronics, ATMEL Germany, project co-ordinator Robert Bosch, Infineon, STMicroelectronics, Philips Semiconductors and X-FAB/Melexis, a software house (Cadence Design Systems), the Fraunhofer Institute IZM and IMEC, and university departments in Bochum, Hanover, Osnabrück, Vienna and Zurich.

ASDESE calls on expertise on ESD and substrate effects from previous work, such as the German parasitic effects in integrated circuits (PARASITICS) project, the EUREKA JESSI AC41 and AC12 projects, and the European Commission ESPRIT EPST and ESDEM projects. The consortium is also co-operating with the MEDEA+ T122 project on the fitness of advanced semiconductor processes for 42V battery supply in automotive applications.

Benefits for Europe

European companies hold a strong position in communications and automotive electronics worldwide. Companies such as STMicroelectronics, Infineon, Philips, Alcatel and Bosch have significant strategic positions in the market, so this project should help to make them, and other European companies, more competitive by reducing mask and silicon processing costs. Time-wasting silicon learning cycles can be reduced, as well as expensive reliability tests.

Simulation models developed and verified within the project will be implemented in a form that can be run in commercially available software tools. ASDESE results should also make a significant impact on international test standards in a field currently dominated by US companies.

Institutions and universities will benefit from deep involvement in industrially relevant problems for future research and education. Undergraduate and PhD students working in the fields of physics, electronic engineering and computer science will receive a welcome employment boost during the project and their skills will become extremely valuable to industry.

MEDEA+ Office
33, Avenue du Maine
Tour Maine-Montparnasse
PO Box 22
F-75755 Paris Cedex 15, France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

EUREKA Σ!

MEDEA+ Σ!2365 is the new industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.