PROJECT PROFILE

T123: Expanding non-volatile memory and analogue functionalities for systems-on-chip (CRESCENDO)

DESIGN METHODOLOGIES

Partners:

IMEC
Infineon
Philips Research
Philips Semiconductors
STMicroelectronics

Project leader:

Frans List, Philips Semiconductors

Key project dates:

Start: January 2001
End: December 2004

Countries involved:

Belgium
Germany
Italy
The Netherlands

Embedded non-volatile memory, low-cost custom programmability and built-in analogue functionality will be essential requirements in future deep-submicron system-on-chip technology for many applications. In the MEDEA+ CRESCENDO project, a consortium bringing together Europe's three top semiconductor manufacturers and leading independent research centre IMEC intends to make advances on all of these fronts, targeting growth market sectors such as smart cards, automotive electronics, consumer devices, multimedia and mobile communications. Starting from previous work on 0.25-μm technologies, project partners will concentrate during the next two years on geometry down to the 0.18- and 0.13-/0.12-μm levels.

The goal of CRESCENDO is to create technological advantage for Europe by enabling system-on-chip (SoC) solutions to be realised through the development of non-volatile and analogue process options in future generation deep-submicron chip technologies.

Partners in the MEDEA+ T123 CRESCENDO project are Infineon, Philips Semiconductors and STMicroelectronics, plus Philips Research and microelectronics research and development center IMEC. Each has a leading role in certain sectors of the market where non-volatile memory (NVM) and analogue devices are a common denominator. CRESCENDO builds on results on previous process generations by the same participants during the earlier MEDEA programme (1997 to 2000).

Series of challenges

The main objectives of the four-year CRESCENDO project are to develop high density non-volatile memory – flash and EEPROM (electrically erasable programmable read-only memory) – as well as low-cost, low-density programming elements, possibly as small as just a few bytes in 0.18- and 0.13-/0.12-μm generation CMOS technologies.

One challenge is to achieve continuing reduction in feature size, while still dealing with the high voltages required for non-volatile memory operation. For true SoC applications, maintaining full compatibility with baseline logic and analogue functionalities is also critical. In addition, the growing demand on interface quality between the external world and the SoC will further increase the need to integrate extremely accurate analogue functions, with respect both to the available voltage supplies and to the integration of different process architectures.

At present, embedded memory is mainly produced using commodity memory processes, which provide high memory density but offer poor logic performance and gate density. For low density memory, a common solution is the use of laser fuse approaches to cope with requirements ranging from parameter trimming and chip identification to implementation of redundancy for embedded dynamic (DRAM) or static (SRAM) memory.

Process technology advances envisaged by the consortium will enable the partners to realise the advanced SoC solutions needed in fast-growing application sectors such as microcontrollers, cellular communications, smart cards, multimedia, automotive electronics and data storage for audio/video.

For instance, the key drivers for the mobile telecommunications market – cost, size/weight, feature density, performance and component count – depend on ever-higher levels of integration and more advanced process technologies. Similarly, multi-application smart cards to be used for a variety of functionalities and services – such as banking, ticket card, pay TV and electronic commerce – will require highly complex circuits incorporating the non-volatile process generation and analogue functions enabled by the CRESCENDO project.

Process innovations

The project is split in two sub-sections. All three semiconductor manufacturers and both research centres are participating in the part covering NVM, while Philips and STMicroelectronics are also involved in the analogue developments.

Innovation goals of the programme are:

• Development of new process modules leading to size reduction in, for example, insulation, stacked gate formation and other characteristics of memory cells;

• Use of alternative programming and erase concepts, together with self-aligned process features, for further memory cell size reduction;

• Introduction of low-voltage programmable elements for low-density memory, making use of alternative programming mechanisms; and

• Digital correction of analogue artefacts in analogue circuitry, and development of circuit techniques that improve performance significantly in terms of bandwidth, power and dynamic range.

The added value of the new processes will be shown by means of demonstrator circuits and analysis of their performance.

Major market potential

Success in these areas will increase European semiconductor companies' capability to adapt their products to market needs, by offering flexible programmability and cutting process costs. Further development foreseen on 0.18-µm EEPROM cell architecture – intended to reduce the writing voltages – will also indicate whether it is worthwhile to extend this cell concept, used particularly in the smart card field, to the next process generations.

The results of the project will have an immediate impact on the partners' own products. Since the option with embedded flash memory has the same performance as the underlying standard logic process, customers will benefit from maximised modularity. Existing logic designs for controller cores of chip-card and automotive applications, for example, can easily be expanded with on-chip NVM modules for data storage and programming functions.

CRESCENDO will deliver technologies that could cover almost all non-commodity applications, for which a greater or lesser degree of NVM content will be necessary. Consequently, its outcomes will also be of significant relevance to a cluster of MEDEA+ Application projects currently underway, in which the availability of appropriate NVM and analogue technology is mandatory.

Available figures indicate that there is huge potential for the new devices in various application fields. It is therefore crucial to offer the technologies involved in this project as soon as possible.

Key enabler for Europe

The market for smart card chips alone, of which Europe forms about 70% and serves about 80%, is expected to triple in size over the project period. Introduction of the proposed embedded NVM technologies will be a key enabler for Europe to capture this and other markets where embedded use is desired for cost, power-saving, size and performance reasons.

In addition, the demand for flash memory will grow strongly. A principal reason for this is the emergence of new applications such as next generation mobile telecommunications, data carriers for mobile audio, and digital camera applications.

'Programmable elements' will open a market that does not actually need full NVM capabilities (at their given cost), but which is looking for a reliable solution to address the increasing demand for products with embedded identification code, trimming and customisation capability. As the SoCs enabled by CRESCENDO could incorporate a definitive answer to the requirement for transaction security, potential sales may be worth billions of euro.

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