MEDEA+

PROJECT PROFILE

T206: CMOS SOI for low power logic and RF wireless (CMOSSOI)

IC TECHNOLOGY INTEGRATION

Partners:

ACP
CEA-DAM
CEA-LETI
Chalmers University of Technology
CHIPIDEA
CISSOID
Ericsson AB
ETH Zuerich
IEMN
IMEP-INPG
Infineon Technologies
Infineon Technologies Wireless Solutions
IXL
Motorola CRC
Philips Research Laboratories
Philips Semiconductors
SARNOFF Europe
SOISIC
SOITEC
STMicroelectronics
Uni Linkoping
Uni Lund
Université Catholique de Louvain
Wacker Siltronic

Project leader:

Eugene Mackowiak
STMicroelectronics

Key project dates:

Start: October 2002
End: September 2005

Countries involved:

Belgium
France
Germany
The Netherlands
Portugal
Sweden
Switzerland

Silicon-on-insulator (SOI) technology has gained a toehold in the semiconductor industry as a fast growing number of chipmakers tap into SOI for device performance gains. Now a substantial group of leading European companies in the SOI market are collaborating to find out whether this technology is suitable for a range of mobile and networking devices and, at the same time, to put Europe firmly in the lead in the race to exploit this technology. MEDEA+ T206 provides its partners with a unique opportunity to research and develop new families of devices that use less power, perform more efficiently and yet are cheaper to produce than current generations of CMOS and high speed BiCMOS technologies.

The requirements for advanced integrated circuits (ICs) to deliver higher speed and performance at minimum power consumption will soon exceed the ability of existing manufacturing techniques with conventional silicon wafers. The number of components integrated on one chip is not limited by area but by power; reducing power consumption has therefore become a critical objective in digital circuit design.

The objective of the MEDEA+ T206 CMOSSOI project is to evaluate, design and manufacture a family of CMOS silicon-on-insulator (SOI) circuits for low-power portable, radio frequency (RF) wireless and high-speed applications to compete with more expensive CMOS and bipolar CMOS (BiCMOS) devices. They must not only consume considerably less power and offer active and passive devices with better RF characteristics, but also be even more reliable and cost-effective to manufacture.

Some manufacturers such as AMD, IBM and Motorola already apply SOI technology to make better use of the silicon wafer surface area and produce high-speed processors based on 90nm CMOS SOI. The role of SOI is to insulate a thin layer of the monocrystalline silicon electronically from the rest of the silicon wafer. Semiconductor manufacturers can then fabricate ICs on the top layer of the SOI wafers, using the same processes they would use on plain silicon wafers.

Higher speeds, lower losses

The embedded layer of insulation enables SOI-based chips to function at significantly higher speeds while reducing electrical losses. The result is an increase in performance and a reduction in power consumption – a major evolution in microelectronics. Huge advances have been made in CMOS SOI technology. The highly integrated nature of CMOS SOI chips provides a cost-effective alternative to gallium arsenide (GaAs) and BiCMOS technology. It also offers design advantages over traditional silicon germanium (SiGe) CMOS technologies, including a significant reduction in cross-talk between RF analogue and digital logic circuitry, and the ability to integrate many different elements easily within the chip. These factors can be enhanced for mixed digital-analogue and RF applications by using high resistivity (HR) substrates with no change in the manufacturing process.

The main semiconductor manufacturers are already evaluating SOI technology for sub-100nm circuits. All are looking at SOI's potential for low-power digital, mixed analogue-digital and RF applications. Intel plans to have thin film SOI devices available by 2005. Texas Instruments is carrying out SOI process research, and Mitsubishi is developing 135 GHz, 70nm CMOS SOI for both RF/analogue and logic applications. Epson, Fujitsu, Honeywell, Lucent, NEC and Philips are also carrying out studies into SOI.

IBM, Sony and Toshiba have announced a major deal to co-develop advanced process technologies for 90nm to 45nm chip designs on 300mm wafer substrates. That partnership aims to move SOI and other advanced semiconductor process technologies into chips for cost-sensitive consumer electronics markets.

Developing process and tools

CMOSSOI will help the European microelectronics industry to develop SOI knowledge, process and tools for low power and for RF applications. Project partners include major SOI wafer manufacturer SOITEC, European silicon wafer manufacturer Wacker and the main European chipmakers. They are evaluating SOI's suitability for various applications. Institute and university laboratory partners are testing the new circuits and seeing how they work with traditional partially depleted (PD) SOI 130nm and 90nm CMOS.

It is also investigating the suitability of fully depleted (FD) CMOS SOI for future sub-90nm devices. For this purpose the project intends to produce ultra-thin single crystal silicon films and simultaneously reduce the thickness of the buried oxide layers on the starting wafers.

Developing 120nm to 90nm PD SOI CMOS for digital, mixed digital-analogue and RF applications and carrying out research into 90nm to 65nm FD SOI devices are clearly state-of-the art and highly innovative processes, so the timing of the CMOSSOI project is crucial if Europe is to remain strong in this field. The SOI substrates specifications need to be adapted to meet the target required for the next, more advanced SOI technologies – such as CMOS RF 120nm technology on HR substrates – and, most of all, for the future sub-90nm FD generations being considered within this project.

The MEDEA+ project will also place European IC manufacturers (Infineon, Philips and STMicroelectronics) in a more comfortable competitive position in which to serve their clients. Ericsson is a world-leading supplier of equipment for telecommunications systems for wired and mobile communication in private and public networks. CMOS SOI technology may have a significant impact on future microwave communication systems because it uses less power, works more efficiently and for less cost compared with today's technologies.

High speed, low power CMOS SOI is expected to be an enabling technology in the development of new communications products for the 10 to 60 GHz frequency band. These systems, such as the 60-GHz wireless local area network (WLAN), will be produced in very large volumes.

Preparing volume production

SOITEC has also become a world leader in the SOI wafer market thanks to its Smart-Cut technology. The recent take-off of industrial SOI applications and announcements of major players in the SOI market – such as IBM in 1998 claiming SOI to be as important as copper interconnects – has put serious pressure on the availability of quality SOI starting material.

If it is to retain its worldwide leadership position and capture market volume, it is very important that SOITEC prepares the next generations of SOI wafers that will be required for future large volume devices well in advance.

From its close contacts with many key customers, SOITEC has identified that for the new generations of SOI, mainly thin and uniform SOI layers are needed, and that such products will dominate the main SOI wafer market segment. HR silicon substrates will appear as an additional option and be targeted at RF applications. SOI substrates in 300mm wafer size will obviously dominate the market in the near future.

Wacker is one of the world's leading producers of electronic grade silicon and a leading wafer manufacturer in Europe. Silicon supply has to adapt to the demand of SOI producers in term of specifications.

Early access for Europeans

Europe will be producing elements for the entire production chain, from silicon wafers to chips on SOI. This project therefore provides a unique opportunity for participants to have very early access to the most advanced SOI wafers available, and to become some of the first main actors on the SOI-based semiconductor technology stage.

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