PROJECT PROFILE

T408: Mask-less mapper (MAPPER)

LITHOGRAPHY

Partners:

IMEC
MAPPER Lithography
Philips

Project leader:

Boudewijn Baud,
MAPPER Lithography

Key project dates:

Start: July 2003
End: December 2005

Countries involved:

Belgium
The Netherlands

Executed by a small university spin-off company, the MEDEA+T408 MAPPER project is aiming at demonstrating the feasibility of a new form of mask-less lithography using hundreds of individually controlled, parallel electron beams to create circuit patterns on the silicon wafer. A production tool with 13,000 beams would be capable of far greater throughput than now possible with electron-beam lithography at the 65- and 45-nm nodes. It could expand the market in low-to-medium-volume fabrication of high-performance application-specific chips and prototyping of large volume devices by making smaller batches affordable. Success will put Europe at the leading edge of high throughput electron-beam lithography worldwide.

Current chip manufacturers create electronic devices by projecting ultra-fine patterns onto a coating of photo-resist on the surface of semiconductor wafers using a microlithography process. The pattern is transferred from a mask onto the silicon wafer using DUV light through an optical-reduction system. Memory chips, microprocessors and other electronic devices with critical dimensions (CDs) as small as 130-nm are now common, 90-nm devices are already in production and 65-nm processes have been proven.

However, as chips become more complex, prices of lithography mask sets are increasing drastically (already reaching €1 million or more). The soaring costs of lithography facing the semiconductor industry pose a serious economic threat to the continuation of Moore's law, stating that the number of transistors on a given area of a semiconductor chip will double every 18 months.

While the fabrication of a complete new mask set could be economically justifiable for high-volume chips, the price of a mask set can push the cost per unit of low volume complex integrated circuits beyond what customers are willing to pay. Because of their limited batch sizes, application-specific integrated circuits (ASICs) – a market where Europe excels – are frequent victims of this economic logic.

Mask-less alternatives

Alternative lithographic technologies are available which do not need a hardware mask. The pattern on the photo-resist coating is written directly using electron beams that receive their pattern information from the data file of the design centre. However, until now, throughput with electron-beam lithography (EBL) has been low. Developments for 130- to 90-nm nodes have generally been limited in throughput to less than five wafers per hour (wph), and in this case only relevant parts of a wafer were exposed. This limit is inherent to current technologies and rapidly decreases to uneconomic values of less than 0.1 wph at 65-nm and below.

The objective of the MEDEA+ T408 MAPPER project is to demonstrate the feasibility of a new EBL concept allowing much higher throughputs. This will reduce the cost of lithography to a level which is also affordable for low volume, complex ASIC products. As a result, the MEDEA+ project will lead to a complete mask-less solution for the lithography market.

For a demonstrator, the MAPPER consortium aims to achieve a throughput at 45-nm equivalent to 1 wph. Subsequent development phases after the feasibility demonstration are planned to achieve a working prototype in late 2006 and a first production tool early 2008. This tool will be able to expose 10 wph with CDs of 45-nm and will be extendable in principle to even smaller feature sizes.

Using parallel beams

What distinguishes the technology proposed by MAPPER from existing EBL tools is the use of massively parallel electron beams, individually switched by light signals. The demonstrator tool will control 100 to 500 beams on an area of 1 x 1 mm^2, while the planned prototype will have 13,000 beams.

With expected throughputs of the order of 1 to 10 wph, MAPPER EBL technology will be economically attractive for batches smaller than 750 wafers per design at CDs of 90-nm, and for batches of less than 1,500 wafers per mask at 65-nm. As a consequence, and after discussions with most major companies in the semiconductor industry, including Philips, STMicroelectronics, Motorola, AMD and Intel, the market for a successful production tool could be 30 units a year, increasing to 90 a year in the longer term.

MAPPER Lithography – a small spin off company from Delft University of Technology, the MAPPER-technology patentee – is leading the project. It is managing its own efforts and those of its four large partners – Philips Enabling Technologies Group, Philips Semiconductors, Philips Research Laboratories and microelectronics research centre IMEC – as well as those of ten subcontractors with excellent records in research, technology development and engineering.

Such co-operation is essential to obtain all necessary knowledge, experience and production capabilities required for this project.

Major subsystems

The major subsystems of the MAPPER tool in this project each focus on a specific project task:

1. The **electron-optics subsystem** – two multiple electron beam columns are being built: one for verification at the subsystem level, and another for incorporation into the demonstrator itself;
2. The **data subsystem** – converting the digital image of a die pattern into switching signals for the electron-beam modulator array. For the demonstrator, the consortium is designing and building a simplified version of the data subsystem required for the prototype. Only 100 channels are planned – sufficient to prove the MAPPER principle and determine what will be required for the 13,000 electron beams planned for the prototype; and
3. The **main control subsystem** – supervising the whole system, translating tool functions into subsystem actions and synchronising the actions of the different subsystems. This is largely a matter of developing software, but is demanding because of the necessity for close collaboration between partners and subcontractors charged with working on the different interacting subsystems.

MAPPER's management team members believe that their extensive experience gained in the space industry, combined with tool building experience from the semiconductor equipment industry, will ease a proper implementation of this project. MAPPER Lithography is performing the system design, integration and testing, resulting in a proof of principle after one and a half years of the two-and-a-half-year project.

Developing new technology

Though the main competitors in mask-less lithography are Advantest and EBeam Corporation in Japan, as well as Leica and Micronic in Europe, a successful development will make possible a serious shift in the market and should lead to increased employment with manufacturing activities for the equipment and subcontracted parts in various European countries. In addition to the technology development, the objective is to maintain Europe's strong position as a major global supplier of semiconductor manufacturing equipment. The vertical co-operation in this project is also ensuring detailed exchange of information, development and analytical results that will further strengthen individual partners' know- how in equipment design, materials, and chip processing.

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