Project result

Energy-efficient devices and energy control systems

Cluster for Application and Technology Research in Europe on NanoElectronics

CA501 | Low-power design approach launches new developer community

Communication-centric heterogeneous multi-core architectures (COMCAS)

Mobile communications are the most important consumer-electronics market worldwide. Yet as features and customer expectations grow, they run up against the same brick wall – battery life. Only by reducing power consumption can manufacturers introduce innovative new features. The challenge for COMCAS was to improve battery life significantly for small-form-factor devices by reducing power consumption. The CATRENE project developed new low-power approaches for semiconductor design which can reduce power consumption by a factor of five. The results are already being exploited in smartphones.

The global market for mobile devices is billions of units a year. Yet the early leadership Europe gained with the GSM mobile phone standard is under attack from Asia and its lower production costs. Innovation is considered key by European companies to maintaining market share; and for mobile devices, particularly smartphones, cutting power consumption is critical.

Such a reduction is crucial because, with a typical modern smartphone, watching a video exhausts the battery within two hours. Most consumer-electronics suppliers – as well as their customers – now consider minimum acceptable battery life between charges to be seven hours, or the length of a typical working day.

The CATRENE CA501 COMCAS project aimed to improve battery life for small-form-factor devices by focusing on low-power solutions for communication-centred multi-core chip architectures. It examined the complete low-power design hierarchy, including systems-level choices, modelling of applications – algorithms and protocols – and architectures, how to maximise reuse of existing intellectual property, partitioning and mapping, virtual prototyping and minimal-power design.

Reducing power use

COMCAS's goal was to reduce total power consumption by a factor of five while maintaining performance at current levels. It targeted 45 and 32 nm CMOS production technologies, building on the results of the MEDEA+ LoMoSA+ project which developed European low-power expertise in homogeneous architectures for mobile and multimedia. The key difference was its focus on communication-centred multi-processor architectures which require new architecture, circuit and software tools to engineer circuits with an unprecedented level of complexity.

The main design innovation was to move from a traditional performance-oriented approach to one in which performance and power consumption were considered in a more integrated manner.

Key elements were:

- Communication-centred run-time configurable heterogeneous multi-core hardware and software;
- Advanced power management at platform level;
- High-level power-estimating tools able to deliver an accuracy of within 20% of actual energy consumption; and

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

ATRENTA
AXIOM-IC
CEA-LETI
CEA-LIST
CNRS [LEAT]
NXP Semiconductors
Recore Systems
STMicroelectronics
ST-Ericsson
Synopsys
Thales
TIMA
TUD

Project leader:

Armand Castillejo
ST-Ericsson

Key project dates:

Start: March 2009
End: February 2012

Countries involved:

France
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	✔
Design technology	✔
Sensors and actuators	
Process development	
Manufacturing science	✔
More than Moore	
More Moore	
Technology mode	45/32 nm

Energy-efficient devices and energy control systems

- Innovative electronic design automation flow and tools.

All these elements needed to be taken into account in an integrated manner if the project was to deliver a significant power reduction.

Underpinning a community

COMCAS met its targets, developing demonstrators for four application domains – video, radio, telecommunications and advanced techniques in 32 nm – confirming the advances achieved. Two demonstrators were shown at the 2011 Nanoelectronics Forum in Dublin, where COMCAS won the first place in exhibition awards. One showed the gains from a new high-performance dual-core processor. The second demonstrator of power characterisation for a programmable architecture resulted in a significant advance for H264 kernel processing using a coprocessor-based accelerator – also known as PraXia – involving a successful collaboration between partners Atrenta and CEA-LIST/CEA-LETI.

The dual-core chip has now been incorporated into a new kit for developers. Snowball is a low-cost, small-form-factor yet powerful mother board for fast development of mobile applications. It combines ST-Ericsson's Nova A9500 dual-core application processor with an innovative MEMS combining a 3D gyroscope, accelerometer, magnetometer and a barometer, GPS, WiFi and Bluetooth features, all in a small battery-operated device. With support for 3D graphics, high definition video and HDMI output, Snowball puts leading-edge video and mobile technologies within reach of a wider community of developers and hobbyists.

Launched at the Mobile World Congress in 2011, Snowball helps software developers to harness the capabilities of the most advanced smartphone and tablet platforms available. It is already leading developers to create applications for Android, Linaro, Meego and Ubuntu, and has given rise to its own open-source developer community, Igloo (**http://www.igloocommunity.org/**).

New market sectors

Partner NXP has been able to develop a near-field communication (NFC) capability for a one-chip design; reduced power consumption enables the chip to handle more NFC data than earlier versions. These capabilities endow chips with important additional features; an NFC-equipped smartphone can be used to pay fares on board buses or trams for example.

NXP also joined with another company in late 2011 to release a NFC-managed online game. Skylanders, already a great success in the USA, enables gamers to keep their own personalised character and environment on a small, easily portable NFC device, and to enter or leave an online game at any location simply by passing the device through the terminal field.

COMCAS also led to several the patents – NXP filed one patent and ST-Ericsson filed two – in particular on power-efficient branch predictions and improved scalar distribution in an SMID system – while UPV filed one on on-chip communication and LEAT filed one on multiprocessor low-power schedulers.

Overall the results will help consolidate Europe's position in the aggressive and fast-growing smartphone market while enabling companies here to attack new radio and video segments – particularly video surveillance.

Finally, the COMCAS results led to a proposed new CATRENE project, BENEFIC, to determine the best energy-efficient solutions for low-power design. BENEFIC is expected to maintain the effort on power reduction through energy harvesting.

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
Tel.: +33 1 40 64 45 60 - Fax: +33 1 43 21 44 71
Email: catrene@catrene.org
http://www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.