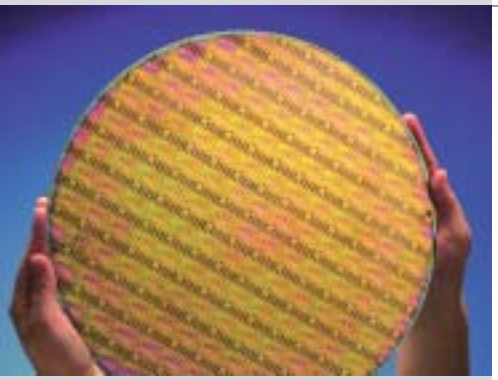
PROJECT RESULT

IC technology integration

MEDEA+

T207: 65 nm CMOS process in 300 mm wafer (65nm CMOS300)



Keeping wafer production well ahead of the field

Close co-operation between major chipmakers, their materials and equipment suppliers, and research centres in the 65 nm CMOS300 project has ensured production of integrated circuits on 300 mm wafers at the 65 nm node level is now possible ahead of the international roadmap and well in time with US and Asian competitors. In addition to boosting the position of materials and equipment suppliers, the results have encouraged collaboration between all leading European chipmakers and research centres for the next stage of chip-processing research – crucial for future competitiveness and employment.

As demand persists for ever more functions in yet smaller electronic systems, there is continuing pressure on chipmakers to shrink processes and put more transistors on the same silicon surface. Technology in production can already scale down below 90 nm half-pitch; the next generation will require 65 nm half-pitch to provide complex system-on-chip designs specified increasingly by the chipmakers themselves rather than their customers. Devices using 90 nm technology are now in full commercial production with applications in communications, consumer electronics and aerospace. The international technology roadmap for semiconductors (ITRS) indicates 65 nm technology is needed for volume production by 2007. It is therefore essential that European chipmakers are able to produce high performance devices with low power consumption using this technology.

The MEDEA+ T207 65 nm CMOS300 project brought together three chipmakers and two research centres as well as the materials and equipment suppliers involved in manufacture to study and develop the new materials, modules and machines necessary to integrate a full 65 nm CMOS logic process. While work started on 200 mm wafers, the main goal was integration of the process in a 300 mm wafer diameter facility; therefore manufacturability on 300 mm wafers and their process-related industrial aspects received the highest attention.

Keeping competitive edge

To keep ahead of global competition, the project had to move fast. Activities were split over five work packages:

1. **Lithography** – optical lithography investigations started with work on new 157 nm wavelength technology but this was quickly stopped as use of existing 193 nm equipment was extended satisfactory to the 65 nm node using both immersion and dry techniques. Good critical dimension uniformity, improved overlay performance and reduced defect density enabled the results of this work to be transferred into production. Alternative electron beam direct write lithography was also studied and showed good potential for prototyping and small series production;
2. **Front end of line** – a major problem was the availability of chemical precursors for high k materials offering the required reactivity and high purity. Two suppliers were involved in improving the chemicals and ensuring cleanliness in production. As a result of this work, Air Liquide is now able to supply advanced precursors and systems for production of 65 nm nodes and beyond, while Epichem is already able to develop the more advanced precursors require for future 32/22 nm nodes in addition to existing products. Work was also carried

out on high k materials and on shallow trench insulation (STI), with consolidation of the STI module developed in the initial part of the project that evolved to a production process;

3. **Back end of line** – extensive studies on different materials and on alternative ultra low k (ULK) deposition provided a good knowledge on porous materials and their integration capabilities. Reliable single damascene additive patterning copper interconnects were achieved on ULK material structures with minimal increase in the effective k value;
4. **Full process integration** – overall a coherent platform was defined for 65 nm CMOS with mature integration results in terms of transistor gates, SRAM memory cells, back-end performance, reliability and yield in line with the requirements of the individual product plans of the industrial partners in the project; and
5. **Test chip and demonstrator** – a design test chip was produced by the chipmaking partners and 65 nm versions of two Bull functional central processing units – cache controller and first level cache memory – were designed.

Technology choices confirmed

Overall, the project has been highly successful with the technology choices made for the 65 nm process well in line with trends in the global semiconductor industry. The process was frozen in early 2005 with the demonstrators run, tested and evaluated. Significant yield improvements were obtained and reliability met specifications, showing all project goals were achieved.

Production on 300 mm wafers was started on the pilot line of the Crolles Alliance – a joint venture in France between project partners STMicroelectronics, Freescale and Philips Semiconductors. The Belgian research centre IMEC and the French research centre CEA-LETI also had technical capacity to work on wafers of this diameter in advanced CMOS technology.

Following the end of the project, the three chipmaking partners are sharing their 65 nm cell libraries and intellectual property blocks but developing and prototyping their own products, mainly for communications. Global competition is tough with at least three companies going into production with 65 nm technology: Intel with microprocessors, Samsung with SRAM, and UMC.

By mid 2006, Freescale had already qualified 65 nm silicon-on-insulator (SOI) technology with two customers. And STMicroelectronics was prototyping customer designs, its own designs and hybrid customer/chipmaker products based on STMicroelectronics' designs but with customers' proprietary cores.

Collaboration set for future

Even more importantly, the MEDEA+ T207 project has created great enthusiasm in the European microelectronics industry and encouraged additional partners to participate in the programme to develop the next technology step: 45 nm. All the major European chipmakers together with the main research centres – IMEC, CEA-LETI and Fraunhofer CNT – will now be working together in a co-operative venture that is crucial for the future of the European microelectronics industry.

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PARTNERS:

Air Liquide
Aixtron
ASMI
Bull
CEA-LETI
Epichem
Freescale
IMEC
LAHC
Lamers
LMGP/INPG/CNRS
LTM/UJF
NXP (Philips Semiconductors)
STMicroelectronics
Vistec

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KEY PROJECT DATES:

Start: January 2003
End: December 2005

COUNTRIES INVOLVED:

Belgium
France
Germany
Italy
The Netherlands
United Kingdom

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.