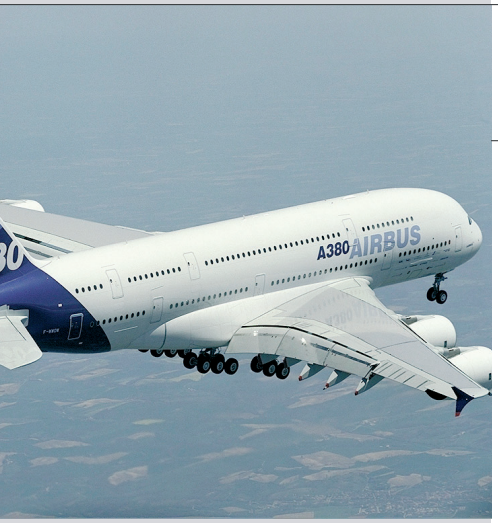
PROJECT RESULT

Design methodologies



A509: Microelectronic EMC system design for high density interconnect and high frequency environment (MESDIE)

Overcoming electromagnetic compatibility issues key to future chip design

Close co-operation between major European chipmakers, electronic design automation (EDA) specialists, systems designers and end-user industries now makes it possible to build more compact equipment with fewer electromagnetic failures but higher performance in a wide range of applications, including automotive electronics, aerospace, telecommunications and consumer electronics. This project has resulted in new EDA methods, models and simulation tools enabling suppliers to design products faster and more efficiently, cutting time to market in key product areas and boosting Europe's global competitive position.

By 2010, integrated circuits (ICs) should have reached 10 GHz clock frequencies, while characteristic design dimensions on chip will have reduced to 45 nm. At the same time, overall chip area will have increased with edge lengths greater than today's 20 mm. There will also be wide use of complex system-on-chip (SoC) devices.

Building ever more compact and faster electronic systems runs increasingly into physical limitations caused by electromagnetic compatibility (EMC) issues, and the difficulty of integrating components into the final design. The need is to improve design methodology and develop modelling techniques to simplify simulation of circuit performance and avoid electromagnetic incompatibilities at an early stage, reducing overall design time.

The basic goal of the MEDEA+ A509 MESDIE project was to close the gap between IC level design and application at system integration level using electronic design automation (EDA). This required development of hierarchical system design approaches and high density interconnect (HDI) technology as well as their introduction for industrial use. New EDA methods enable higher performance and more compact electronic equipment with improved electromagnetic behaviour, and reduce time to market for new devices.

Achievements at all levels

The results achieved cover IC, packaging-interconnect, module and system modelling for tool and EDA environment levels. Highlights include:

- New global simulation strategies for fast EMC simulations and noise analysis offer efficient modelling and analysis for the simulation of emission behaviour in complex digital chips. Model parameterisation was validated by measurement on test chips in 180, 130 and 120 nm technologies. Robust new EMI building blocks were developed for analogue applications and a 40 V smart power application realised in a 0.35 µm technology.
- Three-conductor modelling for improved behaviour at packaging-interconnect level makes it possible to determine correct current return paths and identify discontinuities. The effectiveness of this method was proved in a low-cost, two-layer ball grid array (BGA) flip-chip package. It is possible to optimise transmission paths between IC pads and BGA contacts, minimise cross influences between core and peripherals, and achieve enhanced electrostatic discharge (ESD) and thermal performance.
- A near-field scan approach developed for emission measurement in chip characterisation at module level allows identification of

field distribution above complex IC and HDI structures such as microcontrollers with peripherals. A 'deconvolution' algorithm was introduced to improve the International Electrotechnical Commission (IEC) standard calibration method that enables localisation and detection of parasitic effects in complex microelectronic systems.

- EMC validation at system level in a demonstrator using a new software package was aimed at avionics as new planes require gigascale integrated microelectronic systems in high density packages. Signal paths were analysed in high density package and interconnect structures in an Airbus A380 control unit. Results were fed back to system designers prior to fabrication to achieve low parasitic emissions.
- New multilayer HDI telecommunications systems were designed and implemented with improved impedance and optimised distributed power grid systems.

Advanced tools developed

Advances in the tool and EDA environment included definition and implementation of a platform-independent EMC view at IC level. Three model complexity classes have been introduced. All views consist of equivalent current sources (ECS), based on models for current activity in complex digital modules at chip level.

In addition, methodologies and algorithms were elaborated for analysis of parasitic characteristics of supply systems in complex HDI structures at module level. This makes it possible to calculate the local distribution of the current density in the power system, allowing appropriate design actions to be taken early in development. The algorithms will be integrated in an innovative EDA product from consortium partner Zuken.

A new tool was also developed for automated ESD analysis, offering fast validation of design for automotive applications. This was integrated into a commercial framework for IC design.

High frequency modelling

Higher processing speeds, greater memory capacities, lower power consumption at lower logic voltages and much increased integration all mean EMI parasitic effects in chips will continue to grow. Use of high-frequency EMC modelling is therefore critical, as defined in the 2005 International Technology Roadmap for Semiconductors (ITRS) and the 2005 MEDEA+ EDA Roadmap. Both roadmaps indicate increasing need for high-frequency analysis, simulation and modelling at chip, package and subsystem levels. Reasons are, for example, multi GHz signal bandwidths at all levels of integration and packaging, mixed analogue, digital and radio frequency signal functionality, and greater wiring densities in complex 3D environments.

More than 140 publications and presentations, filing of ten patents, contributions to standardisation bodies and organisation of EMC-specific workshops and seminars ensured wide dissemination of results. The breadth of the consortium that included chipmakers, systems designers, equipment manufacturers, research centres and academia, tool vendors and end-user industries ensures results will be applied in industrial fields key to Europe's competitive future: automotive, aerospace, communications and consumer electronics. Enhanced products from EDA tool vendors are an additional success.

Design methodologies

A509: Microelectronic EMC system design for high density interconnect and high frequency environment (MESDIE)

PARTNERS:

Alcatel
Conti TEMIC
EADS
Gesellschaft zur Förderung angewandter Informatik (GFaI)
IMST
Infineon Technologies
Magneti Marelli
Philips
Robert Bosch
STMicroelectronics
Uni Paderborn
Zuken

PROJECT LEADER:

Werner John
Fraunhofer Institute

KEY PROJECT DATES:

Start: January 2001
End: May 2005

COUNTRIES INVOLVED:

France
Germany
Italy
The Netherlands

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

EUREKA Σ!

MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.