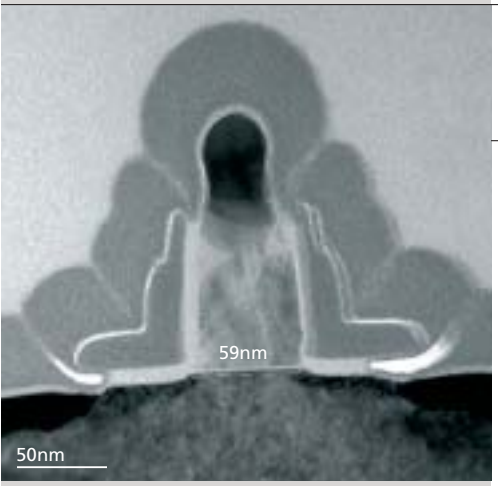
PROJECT RESULT

IC technology integration

MEDEA+



T201: CMOS logic 0.1 μm and below (CMOS logic 0.1μm)

Successful process integration set to boost chip performance

As node size reduces, the number of active devices on a chip can be increased – so boosting performance. With production of sub-100nm devices scheduled for 2003, the MEDEA+ T201 project set out to integrate all the modules required for such fabrication. Design rules were ready for the full 90nm process at the end of 2002 – and preparatory work for the 65nm process was well advanced. The project covered lithography, improved substrate materials and metallisation, and device architecture optimisation. This technology will help keep European semiconductor manufacturers in the top ten worldwide.

Led by semiconductor manufacturer STMicroelectronics, the MEDEA+ T201 CMOS logic 0.1μm project brought together major European chipmakers, process equipment manufacturers, materials suppliers and research institutes. Although the original target was to develop the process for the large-scale fabrication of 100nm devices, the project quickly adapted to the smaller 90nm feature sizes identified as the next technology node by the revised International Technology Roadmap for Semiconductors (ITRS) in 2001.

The objective of the project then became to integrate the 90nm CMOS technology process and to characterise the process modules for physical gate lengths down to 65 nm and below through embedding of these modules in the 90nm process.

Process development and material optimisation

Use of phase-shift masks and optical proximity correction (OPC) made it possible to obtain good process window and very good critical dimensions control even down to 65nm gates using 193nm optical lithography. Gate patterns were also successfully processed with electron-beam direct writing in close to real process conditions to anticipate module development before the optical lithography techniques were made available.

Although extensive tests were carried out on high-k dielectrics – mainly hafnium oxide (HfO_2) and its derivatives – with promising electrical results, the 90nm process was finally integrated by making use of oxinitrides as gate dielectrics. Shallow trench isolation (STI) processing was also optimised for the front-end CMOS integration – the front-end covers all the steps from the initial pure silicon to the fabrication of transistors.

The back-end covers the connections to transistors and subsequent layers of metallisation. Extensive studies were carried out on the development and integration of back-end CMOS modules with low-k dielectric films based on organic SiLK semiconductor dielectric resin and carbon-incorporated silicon oxide (SiOC). SiOC was selected for further work on integration and problems of resist poisoning were resolved, making it possible to demonstrate integration of SiOC in back-end processing.

Metallisation layers provide interconnections between the individual on-chip devices. In the 90nm CMOS process, there may be up to eight layers. In the T 201 project, double-metal, dual-damascene interconnects for up to six copper layers were fabricated and characterised with good

electrical performance. The damascene process involves delineating metal interconnects in the dielectrics separating them, filling the resulting 'trenches' with the metal and removing the excess by chemical mechanical polishing.

Full CMOS process integration required optimisation of transistor architectures to achieve performance specifications and demonstrate basic functional circuits. The 90nm platform consists of two core transistor families and input/output devices. A fully functional 1Mb SRAM was successfully demonstrated.

Design rules for 90nm CMOS were finally issued in the last quarter of 2002 with a demonstrator from computer manufacturer Bull being fabricated at the beginning of 2003 – an essential step to full implementation of the integrated process for volume production. This chip had 54 million transistors, 300 million contacts and over 9 km of interconnects.

Competing in a global market

Success in the MEDEA+ T201 project has been vital to keep Europe on centre stage in a global microelectronics market. Such achievements in this sector are very much a question of timing, and the consortium's customers are already demanding this technology.

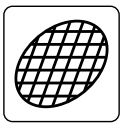
The main two chipmaking partners in the consortium, Philips and STMicroelectronics, are now at the same technology level as their worldwide competitors. Prototype production has already started and they will produce 90nm technology devices using 300mm diameter silicon wafers. This will be one of the most advanced fabrication processes in the world.

Crolles in France, where Philips and STMicroelectronics have a major collaborative research operation together with Motorola that recently joined the team, is an important and growing centre for the semiconductor industry. Many support companies have set up operations in the area, and this in turn is attracting further companies and highly skilled engineering professionals.

Leica carried out key work on electron-beam lithography equipment, which was used as part of the process to anticipate module development and the first demonstration. Electron-beam direct writing is not usually satisfactory for production environments but the project found that, when used in conjunction with optical lithography, acceptable yields were produced. Another partner, Aixtron, developed high-k materials and precursor gases for the chemical vapour depositions processes used to form the transistor gates.

Collaboration key to success

All the consortium members agree that the two-year project has been highly successful. Co-operation has been excellent, both horizontally between semiconductor manufacturers, and vertically within the value chain. The MEDEA+ framework was of great assistance. There is a pool of companies and institutions that work in the MEDEA+ arena, and very often this is where prospective partners first meet. MEDEA+ provided sound advice in a number of areas and advised, for instance, on how best to enter into negotiations with respective national governments for funding.



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Partners

Air Liquide
Aixtron
Bull
Epichem oxides and nitrides
IMEC
INPG/CNRS
Jobin Yvon
Leica Microsystem Lithography
LETI
LTM/CNRS
Philips
STMicroelectronics

Project leader

Guillermo Bomchil,
STMicroelectronics

Key project dates

Start: January 2001
End: December 2002

Countries involved

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France
Germany
United Kingdom

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.