PROJECT RESULT

Process equipment

T303: Contactless anneal and silicides system (CLASS)

Rapid thermal processing boosts European chipmaking

Annealing is a key step in the fabrication of semiconductor wafers. The MEDEA+ T303 CLASS project combined European expertise in equipment design, materials knowledge and chip processing to develop a revolutionary process where heat transfer takes place through conduction rather than radiation. The wafers are located very precisely between two graphite blocks in a stream of hot gas, ensuring the material is heated rapidly and uniformly. The results of this project provide Europe with a global lead and should boost manufacturing employment in equipment and subcontracted parts across the region.

CLASS set out to investigate the development of equipment and processes for annealing – a vital stage in the fabrication of advanced semiconductor structures. Sharp rises and falls in temperature are needed to achieve good quality and yields. Conventional annealing uses heat radiation from tungsten filament lamps to heat wafers. The project was started by ASM as it was close to its core business of thin film deposition. The consortium has a high vertical integration. Xycarb, for example, manufactures refractory (i.e. high temperature) materials and developed the silicon carbide (SiC) that coats the graphite blocks. Research institutes CEA-LETI and IMEC installed alpha-systems for process development and comparison with lamp-heated systems. Major chipmaker STMicroelectronics is at the top of the integrated supply chain.

Three annealing processes

CLASS targeted the 100-nm CMOS process initially, but redefined its objective as the 65-nm node in the course of the project. It focused on three approaches:

1. Spike annealing of low-energy ion implants in very short high-temperature processes to recrystallise the silicon single crystal and to avoid diffusion of dopants deeper into bulk. This is the most demanding approach and was seen as the most likely to benefit from the improvements brought about by CLASS. It was demonstrated successfully on 65-nm devices, resulting in improved performance;
2. Silicidation of both cobalt ($CoSi_2$) and nickel (NiSi) for gate electrodes and source/drain areas – this achieved similar quality and yields with $CoSi_2$ and, in the case of NiSi, improved performance relative to existing annealing processes; and
3. Rapid thermal oxidation – a satisfactory solution was not achieved during the project as no heating blocks could be found to operate in 100% pure oxygen.

Previously, the method commonly used to produce rapid temperature rises was to heat the semiconductor wafer with a tungsten lamp. Many aspects make this less than satisfactory: the thermal efficiency is only 5 to 10%, the rate of heating is relatively slow – not exceeding 250°C/s – and heating depends on the optical properties of the wafer surface.

CLASS uses conduction for heat transfer. The wafer passes through the gap formed by two massive blocks of graphite heated to the required temperature. Jets of high-pressure gas flood the gap through many small-bore holes in the graphite. This creates a

very precise hot-air cushion upon which wafers can float. For this reason the system is called 'Levitor'.

The process has many advantages compared with the lamp method:

- Rate of temperature change is very rapid at 900°C/s;
- Heating is uniform;
- Temperature control is simplified; and
- It is insensitive to the optical characteristics of the material.

Rapid cooling can be effected the same way. Circulating water through plates of the cool-down unit achieves a cooling rate exceeding 400°C/s. Rapid cooling is important to avoid phenomena such as transient-enhanced diffusion of boron. The system can operate from 200 to 1100°C.

Reduced power consumption

Process power consumption is between 6 and 20 kW – a marked improvement compared with the tungsten lamp method that consumes 200 to 250 kW. The SiC-coated graphite blocks act as a thermal flywheel; thermal efficiency is estimated as 65%. Furthermore, the operating cost of the graphite blocks is less than the tungsten filament lamps that need to be replaced regularly. This contributes to the lower running cost of the Levitor system. An objective was for Xycarb to develop blocks of solid SiC, an extremely durable material; prototypes are ready for testing. The CLASS method can handle 75 wafers an hour for one module, a big improvement over other systems. As production of a wafer of logic and memory chips may require between 10 and 15 annealing cycles, the commercial outlook is good.

The alpha-systems at LETI and IMEC were for 200-mm diameter wafers; a tool for 300-mm wafers was also developed as part of the project, requiring manufacture of larger SiC-coated graphite blocks. Processing 300-mm wafers was an important goal because it more than doubles the number of chips per wafer compared with 200-mm wafers. The gap between wafer and blocks has to be carefully controlled: the blocks must be perfectly flat to within 20 microns for the system to heat uniformly.

STMicroelectronics applied the spike-anneal process to develop basic 65-nm CMOS technology in Crolles (FR). It is evaluating the 300-mm Levitor system for the 65-nm technology node. The system was used in the formation of ultra-shallow junctions, producing devices with reduced short-channel effects but a slightly lower drive current compared with the best lamp-based annealing. Furthermore, it has also been applied to form NiSi on source, drain and gate areas of the transistors.

Competitive advantage

The target markets for wafers developed using this process are mainly communications and consumer electronics. The system will provide a competitive advantage for the 65- and 45-nm processes advocated by the International Technology Roadmap for Semiconductors (ITRS). It has already been qualified for 65 nm, and qualification for 45 nm is commencing. Commercially, the system is now marketed worldwide, and complete systems are available.

In the longer term, the CLASS system will reduce the cost of fabrication and enable even more functionality to be put on silicon. This will lead to innovative applications that will open up new markets – good news for the employment, prosperity and competitiveness of Europe as a whole.

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Partners

ASM International
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IMEC
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STMicroelectronics
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Key project dates

Start: January 2001
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Countries involved

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